PVP 14

Code: CS2T4

I B.Tech - II Semester – Regular Examinations – JULY 2015

DIGITAL LOGIC DESIGN
(COMPUTER SCIENCE & ENGINEERING)

Duration: 3 hours Max. Marks: 70

PART – A

Answer ***all*** the questions. All questions carry equal marks

11x 2 = 22 M

1. a) Why NAND and NOR are universal gates?

   b) Determine the value of base if $(225)_x=(341)_8$

   c) Convert the following into equivalent binary value

   i) $(AC3D)_{16}$ ii) $(32AC)_{16}$

d) Explain the terms: Implicant, Prime Implicant and Essential Prime Implicant.

e) Define combinational logic and give one example.

f) What do you mean by comparator?

g) Implement half subtractor using NAND gates only.

h) Difference between PLA & PAL.

i) Differences between synchronous and asynchronous counters.

j) How many flip flops are required for Mod-M counter?

k) Which logic gate is used in parity checker?

PART – B

Answer any ***THREE*** questions. All questions carry equal marks. 3 x 16 = 48 M

2. a) Convert the following number from the given base to other three bases indicated:
Decimal 52.45 to binary, octal and hexadecimal. 7 M

b) Simplify the Boolean function F and implement using NAND gates, use the Don't-care conditions d, in (i) sum of products and (ii) products of sums

$F = \overline{A}\overline{B}\overline{D} + \overline{A}CD + \overline{A}BC$, d= $\overline{A}B\overline{C}D + ACD + A\overline{B}\overline{D}$

7 M

c) Define Arithmetic overflow and give one example. 2 M

3. a) Simplify the following Boolean equation
Y(A,B,C,D)=(A+C+D) (A+C+$\overline{D}$) (A+$\overline{C}$ +D)(A+$\overline{B}$) 8 M

b) Realization of given Boolean expression using universal logic(NAND & NOR)
F=C$\overline{C}\overline{D}$ + $\overline{B}\overline{D}$ + $AB\overline{C}$ + $\overline{A}BCD$ 8 M

4. a) Design a combinational logic circuit with four input lines that represent a decimal digit in BCD and four output lines that generate the 9's complement of the input digit. 7 M

b) Implement a full Adder using two 4:1 multiplexers. 5 M

c) Design 4-bit to 2-bit priority encoder. 4 M

5. a) Realize the following equations with a suitable PLA. Draw the logic diagram using PLA.

$F_1(A,B,C,D)=A\,\overline{B}\,D+A\,\overline{A}\,B\overline{D}$, $F_2(A,B,C,D)=A+B\,\overline{D}$ 8 M

b) Design a switching circuit that converts a 4-bit binary code into a 4-bit Gray code using ROM array. 8 M

6. a) Design a conversion logic to convert JK flip flop to SR flip flop. 8 M

b) Design a Mod-12 synchronous counter using JK flip flops. 8 M